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PRODUCTION

Selling Time without Compromise

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In this world of shortening product cycles and highly competitive markets, faster time-to-market is essential. At Quik-Pak, a division of Delphon Industries, we know all too well what it means to "sell time" in the Semiconductor Industry without compromise to quality or workmanship. Selling time requires a significant amount of ingenuity, creativity, and flexibility to ensure a product is ready to ship to the user within a matter of a few days or even within a few hours.

At the end of an intense product design project and several weeks of wafer fabrication, the last steps to complete prototype integrated circuits are packaging and test. By the time these first wafers are ready for packaging, there is intense pressure to quickly validate whether the design works to specification. With the competitive market driving the need for innovative products, more design engineers, product managers and packaging professionals are seeking packaging methods to test new devices or concepts quickly without a significant amount of expense.

Open Cavity Process

So how does Quik-Pak "sell time"? One way is through the company's patented Open Cavity IC Plastic Packages (OCPP) process. The process utilizes mechanical samples, test rejects, or excess inventory to create an open cavity package. The die pad and lead fingers are exposed for easy assembly of various pin counts and body sizes for MLF, QFN, MLP, LPCC, DRN, BGA, QFP, SSOP, TSOP, PLCC, SOT, SOIC, SOJ, etc. The OCPP possibilities for enabling IC design verification are endless, and they result in a chip assembled in a package that is electrically and physically equivalent to that which will be used in final production.

Quik-Pak's open cavity packages can be encapsulated in various options depending on the user's requirements. Many users are satisfied with a standard glob top, but others require testability within the JEDEC Standards for package outline. Since standard glob top packages are not compatible with many test sockets, Quik-Pak engineered a patented method for flattening and remolding of open cavity packages. This can be applied to any packages, making them suitable for socket testing, automatic handling, and marking of pre-production packages.

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In some cases, permanent encapsulation is not feasible for a given application, since the IC designer needs to gain access for additional probing or FIB (Focused Ion Beam) work. The solution to protecting the chip during transport and internal handling while still maintaining access to the chip is utilization of a perimeter frame and lid. As frames and lids for the wide variety of packages are virtually non-existent in inventory or on the open market, Quik-Pak's engineers design and laser-cut custom frames and lids from various materials such as FR4 or Kevlar.

During the package preparation, the frames are secured to the packages and are ready for die assembly. Once the die are attached and wirebonded or studbumped, the lids are glued to the frames to protect the die. The lids can be easily removed to gain access to the die for inspection, circuit repair or any necessary probing required. This is also an ideal solution for many MEMS applications.

Creative Ways to Enable Design-Ready Package

In some cases, there is not a ready supply of packages available to meet the needs of special applications. When time is critical, Quik-pak seeks creative new ways to enable a design-ready package in only a few days. One particular example is a power DFN packaging requirement. Time was of the essence and the chip design required 8 connections, but only a 3-leaded DFN was available on the open market to support the given device parameters. Within a few days, the 3-leaded DFN was transformed into an 8-leaded DFN. This package transformation could only have been achieved by utilizing the Quik-Pak open cavity package process.

This process allowed clean access to the existing die pad and lead fingers. With all internal leads and existing pads exposed, Quik-Pak laser-cut the existing leads and die paddle using a custom Yag Laser system to transform the existing 3-lead package into 8 leads and a new die paddle. Once the new die paddle and leads were reformed, the package was remolded to form a rigid body for package assembly. The new 8-lead DFN was gold-plated to ensure bondability. Within a week after the initial request, the company created and assembled the new 8-lead package for rapid design verification. This process of reforming an existing power DFN not only saved the customer over eight weeks and tens of thousands of dollars, but the customer also had test-ready packaged devices in half the time it would have taken to tool a new package.

Whether it's an unexpected delay with a design tape out and wafer fabrication or a special application, IC Designers and Product Engineers continue to take advantage of the full turnkey solutions available at Quik-Pak. From wafer backgrinding, saw and dicing, all the way to chip assembly and packaging, our enables customers to turn an idea into reality within a matter of hours.

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